## Laboratory Report Cover Sheet



#### Name :

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment :**

**Date of Conduction :**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

**3. Implementation of a Sequence detector circuit**

**Aim:** To design and implement sequence detector circuit

**Software requirements:** Logisim

**Theory:** A sequence detector

is a sequential state machine which takes an input string of bits and generates an output 1 whenever the target sequence has been detected. In a Mealy machine, output depends on the present state and the external input (x). Hence in the diagram, the output is written outside the states, along with inputs. Sequence detector is of two types:

Overlapping

Non-Overlapping

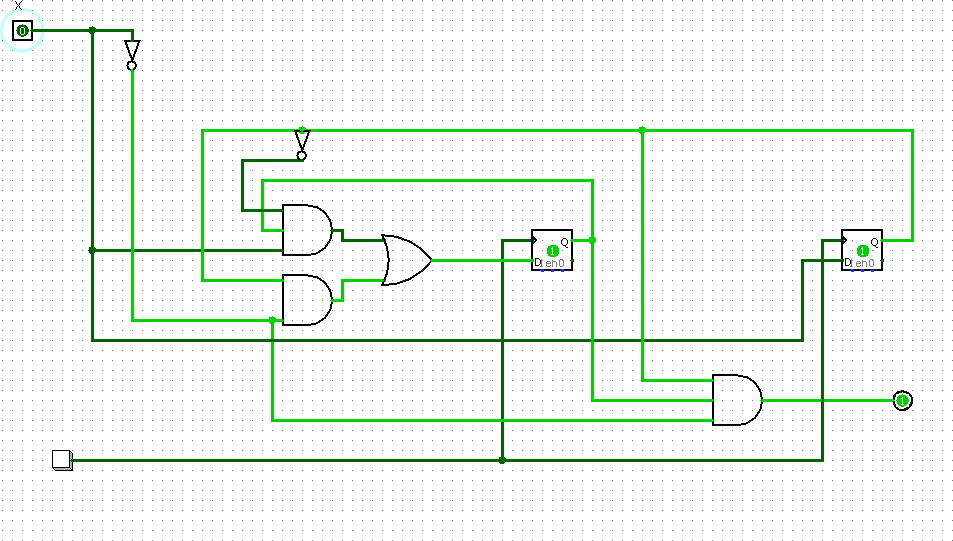
In an overlapping sequence detector, the last bit of one sequence becomes the first bit of next sequence. However, in non-overlapping sequence detector the last bit of one sequence does not become the first bit of next sequence.

Problem statement: Design a sequence generator using Mealy machine to check the following sequence 1010 using D flip Flop

0/0

1/0 0/1

**Fig.4 State Diagram for 1010 sequence detection**



**Fig.5 Logic Diagram for sequence detector**

**Pre-lab questions:**

1. Discuss on Mealy and Moore state machines.
2. Draw the Moore FSM for 10X1 and explain.
3. Draw the Mealy state diagram for 11011 sequence detectors with and without overlap

**Post-lab questions:**

1. Give the applications of sequence detector.
2. (i)Design a Mealy sequence detector to detect a sequence 1011. (ii)Implement the above sequence detector using D flip flop and logic gates.

**Result:**